SIE 370
Embedded Computer Systems
Spring 2016

Class Hours: Tuesdays and Thursdays at 1:00 - 2:30 PM
Lab Hours: Wednesdays at 2:00 – 5:00 PM
Classroom: ET 127
Laboratory: ET 128
Instructor: Samuel Peffers, ET 122, (928) 317-7067, samuelpeffers@email.arizona.edu
Office Hours: M,W, F 9:00 – 11:00 AM, or by appointment

**Course Description**: Boolean algebra, combinational and sequential logic circuits, finite state machines, simple computer architecture, assembly language programming, and real-time computer control. The computer is used as an example of systems engineering design; it is analyzed as a system, not as a collection of components. There is a lab associated with this course.

**Prerequisites**: ENGR102 and ENGR 211M or ECE 207, or articulated equivalents.

**Course objectives**:
1. Understand number systems, Boolean algebra, Karnaugh maps, and digital logic design program so that you can design, build and test digital circuits.
2. Know how to devise a state machine to describe the actions of a microcontroller based system.
3. Understand how to translate a software implementation of a system into a hardware implementation or vice-versa.
4. Construct actual microprocessor systems using integrated circuit devices, clocks, and other electrical components.
5. Know how to analyze a problem that can be solved using a digital logic system and successfully design that system.

**Textbooks** and other materials are all available on D2L, there are no course specific materials required for this course; D2L is the primary means of distributing class material.

**Academic Integrity**: The University's policy on academic integrity is available at the link below. I fully support and actively enforce this policy. As mature adults, professionals, and scholars, this should not be an issue in this course. If you have questions regarding this policy, raise them with me immediately.

http://catalog.arizona.edu/policies/974/acacode.htm

**Special Needs**: The American with Disabilities Act of 1990 requires universities to provide a "reasonable accommodation" to any individual who advises us of a physical or mental disability. If you have a physical or mental limitation that requires an accommodation or an academic adjustment, please contact me at your earliest convenience.

**Changes and Addenda**: As circumstances require, the instructor may publish addenda or changes to this syllabus and other related course material. In such a case, students will be asked to acknowledge receipt of the addenda or changes as applicable.

**Assessment and Deliverables**:

| Product | Percentage of Course Grade | |
|---|---|---|
| Mid-term Exam | | 15% |
| Final Exam | | 20% |
| Quizzes / Homework (highest five scores) | | ea. 2% |
| Lab Products & Reports (ten scores) | | ea. 1% |
| Term Project | | |
| Proposal | | |
| | Written | 3% |
| | Oral | 2% |
| Requirements Validation Review (RVR) | | |
| | Written | 3% |
| | Oral | 2% |
| Preliminary Design Review (PDR) | | |
| | Written | 3% |
| | Oral | 2% |
| Test Readiness Review (TRR) | | |
| | Written | 3% |
| | Oral | 2% |
| Design Acceptance Review (DAR) | | |
| | Written | 10% |
| | Product | 10% |
| | Oral | 5% |

**Grading Scale**:

A: 90 – 100
B: 80 – 89
C: 70 – 79
D: 60 – 69
F: 0 – 59

**Course Schedule**:

| Date | Activity / Topic |
|---|---|
| Jan 14, 2016 | Course introduction, embedded systems and Arduino fundamentals |
| Jan 19, 2016 | The design process |
| Jan 20, 2016 | **Lab 1**: laboratory safety, procedures, simple circuits |
| Jan 21, 2016 | Technical Process 4.1 (Business Analysis Process) |
| Jan 26, 2016 | Digital input to digital output |
| Jan 27, 2016 | **Lab 2**: Digital input to digital output |
| Jan 28, 2016 | Analog input to analog out put |
| Feb 2, 2016 | **Project proposal presentations** |
| Feb 3, 2016 | **Lab 3**: Analog input to analog out put |
| Feb 4, 2016 | Technical Processes 4.2 and 4.3 (Stakeholder Definition Process, and Requirements Definition Process) |
| Feb 9, 2016 | Analog input to digital output |
| Feb 10, 2016 | **Lab 4**: Analog input to digital output |
| Feb 11, 2016 | **Requirements Validation Review (RVR)** |
| Feb 16, 2016 | Digital input to analog output |
| Feb 17, 2016 | **Lab 5**: Digital input to analog output |
| Feb 18, 2016 | Technical Process 4.4 (Architecture Definition Process) |
| Feb 23, 2016 | Technical Process 4.5 (Design Definition Process) |
| Feb 24, 2016 | **Lab 6**: Preliminary Design Review preparation time |
| Feb 25, 2016 | **Preliminary Design Review (PDR)** |
| Mar 1, 2016 | Motor control |
| Mar 2, 2016 | **Lab 7**: Motor control |
| Mar 3, 2016 | **Mid-term Exam** |
| Mar 8, 2016 | Visual display control |
| Mar 9, 2016 | **Lab 8**: Visual display control |
| Mar 10, 2016 | Technical Processes 4.9 and 4.11 (Verification Process, and Validation Process) |
| Mar 22, 2016 | Sensor control |
| Mar 23, 2016 | **Lab 9**: Sensor control |
| Mar 24, 2016 | Finite State Machines |
| Mar 29, 2016 | Multifunctional control |
| Mar 30, 2016 | **Lab 10**: Multifunctional control |
| Mar 31, 2016 | Logical architecture and logic circuits |
| Apr 5, 2016 | **Test Readiness Review (TRR)** |
| Apr 6, 2016 | In lab project build / test time |
| Apr 7, 2016 | Karnaugh maps |
| Apr 12, 2016 | Boolean algebra |
| Apr 13, 2016 | In lab project build / test time |
| Apr 14, 2016 | Systems Modeling |
| Apr 19, 2016 | Systems Modeling |
| Apr 20, 2016 | In lab project build / test time |
| Apr 21, 2016 | Systems Modeling |
| Apr 26, 2016 | Design Acceptance Review discussion / preparation |
| Apr 27, 2016 | In lab project build / test time |
| Apr 28, 2016 | **Design Acceptance Review (DAR)** |
| May 3, 2016 | Review / prepare for final exam |
| May 5, 2016 | **Final Exam** |